CLAIMS

1. A method for controlling an arithmetic codec context, comprising the steps of:

(A) reading a current value indicating one of a first condition and a second condition corresponding to a current context of a plurality of predetermined contexts;

(B) generating an input state matching (i) an initial state in response to said first condition and (ii) an output state in response to said second condition, wherein said initial state has a predetermined value and said output state has a value generated by said method before receiving said current context; and

(C) generating a current output state by performing an arithmetic code operation on an input signal using said input state.

2. The method according to claim 1, wherein step (B) comprises the sub-step of:

generating said input state from a prior output state in response to said current context matching a prior context of said predetermined contexts.

3. The method according to claim 1, further comprising the step of:

setting said current value to said second condition after generating said input state.

4. The method according to claim 1, further comprising the step of:

clearing a plurality of said current values to said first condition substantially simultaneously in response to a clear signal being asserted.

5. The method according to claim 1, further comprising the step of:

storing said current output state as said output state corresponding to said current context.

6. The method according to claim 1, further comprising the step of:

scaling said initial state prior to generating said input state.

7. The method according to claim 1, further comprising the steps of:

generating an output signal by performing said arithmetic code operation on said input signal; and

generating a video signal by decompressing said output signal.

8. The method according to claim 7, wherein said decompressing is compliant with at least one of (i) an International Organization for Standardization/International Electrotechnical Commission 14496-10 standard and (ii) an International Telecommunication Union-Telecommunications Standardization Sector Recommendation H.264.

9. The method according to claim 1, further comprising the steps of:

generating said input signal by compressing a video signal.

10. The method according to claim 9, wherein said compressing is compliant with at least one of (i) an International Organization for Standardization/International Electrotechnical Commission 14496-10 standard and (ii) an International Telecommunication Union-Telecommunications Standardization Sector Recommendation H.264.

11. An apparatus comprising:

a first memory configured to store a plurality of initial states corresponding to one of a plurality of predetermined contexts;

a second memory configured to store a plurality of control values each indicating one of a first condition and a second condition corresponding to one of said predetermined contexts;

a third memory configured to store a plurality of output states each corresponding to one of said predetermined contexts; and

an arithmetic coder configured to generate an output state by performing an arithmetic code operation on an input signal using an input state, wherein said input state matches (i) one of

said initial states in response to a current control value of said control values having said first condition and (ii) one of said output states in response to said current control value having said second condition.

12. The apparatus according to claim 11, further comprising a multiplex circuit coupled to an output of each of (i) said first memory, (ii) said second memory, (iii) said third memory and (iv) said arithmetic coder and configured to generate said input state in response to one of said control values.

13. The apparatus according to claim 12, further comprising a comparator configured to generate a signal to control said multiplex circuit in response to comparing a current context of said predetermined contexts with a prior context of said predetermined contexts.

14. The apparatus according to claim 13, further comprising a scalar circuit disposed between said first memory and said multiplex circuit and configured to scale said initial states read from said first memory.

15. The apparatus according to claim 11, wherein said first memory is configured to transfer one of said initial states in response to both a current context of said predetermined contexts and a signal identifying a current slice within said input signal.

16. The apparatus according to claim 11, wherein said first memory, said second memory, said third memory and said arithmetic coder form a content-based adaptive binary arithmetic coder.

17. The apparatus according to claim 16, wherein said context-based adaptive binary arithmetic coder is configured to decode said input signal.

18. The apparatus according to claim 16, wherein said context-based adaptive binary arithmetic coder is configure to encode said input signal.

19. The apparatus according to claim 16, wherein said content-based adaptive binary arithmetic coder is compliant with at least one of (i) an International Organization for Standardization/International Electrotechnical Commission 14496-10 standard and (ii) an International Telecommunication Union-Telecommunications Standardization Sector Recommendation H.264.

20. An apparatus comprising:

means for reading a current value indicating one of a first condition and a second condition corresponding to a current context of a plurality of predetermined contexts;

means for generating an input state matching (i) an initial state in response to said first condition and (ii) an output state in response to said second condition, wherein said initial state has a predetermined value and said output state has a value generated by said apparatus before receiving said current context; and

means for generating a current output state by performing an arithmetic code operation on an input signal using said input state.